

Notice of References Cited	Application/Control No. 10/716,573	Applicant(s)/Patent Under Reexamination LABERGE, PAUL A.	
	Examiner Jeremy S. Cerullo	Art Unit 2112	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
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FOREIGN PATENT DOCUMENTS

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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	On Slot Allocation for Time-Constrained Messages in Dual-Bus Networks - Ching-Chin Han - IEEE - July 1997
	V	A Pipeline-Based Approach for Maximal-Sized Matching Scheduling in Input-Buffered Switches - Eiji Oki, et al - IEEE - June 2001
	W	A Hard Real-Time Bus Arbitration Protocol based on EIA-709 - Alexander Bauer, et al - IEEE - 2002
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
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